REMARKS

Applicants request further prosecution, entry of the above amendment, and allowance. Independent claims 21, 40 and 42 correspond to the claims made by examiner's amendment that were further amended to more precisely define the step of removing the isolation material from above the gate electrode. Now that step removes enough of the isolation material to leave the top surface of the isolation material proximate to but slightly below the upper surface of the upper layer of the semiconductor substrate. This limitation is supported in the disclosure. See page 5, lines 21-23 and Fig. 2B. The amended step in effect calls for slightly over etching the isolation material layer. The over etching has the beneficial effect of making sure that substantially all of the isolation material is removed from the top surface. That leaves the surface free from spurious, residual dielectric material. After the sources are formed and the metal contacts are made to the source regions, there will be little or no spurious dielectric covering the source regions. Prior art processes could leave such spurious isolation regions on the upper surface of the upper layer. The spurious isolation regions add their resistance to the resistance of the source regions. The over etching step of the invention eliminates most if not all of the isolation debris and provides larger, isolation-free source regions for receiving the source contact metal. The larger the isolation-free source regions, the lower the on resistance.

Applicants have also amended the independent claims to remove the limitation that the gate material is deposited to a selected level. The gate electrode may be formed by selective deposition or by depositing gate material in the trench and them removing it. Such a deposition and etch step is conventional as shown in the Harada reference of record, US 5298780. As such, Applicants withdraw their prior remarks that distinguished Harada from the claimed invention on the basis of the selective deposition of gate material. However, neither Harada nor any other reference shows or suggest the step

of slightly recessing the isolation layer at the top of the trench to increase the source contact area and reduce on resistance.

Accompanying this request is an Information Disclosure Statement that contains three references not of record. One is US 5034785 (Blanchard), another is US 5080795 (Temple) and the third is a translation of JA Publication No. 53:142189.

Blanchard fails to show or suggest the step of etching the isolation layer below the upper surface of the upper layer. See Fig. 7 of Blanchard and the dimple 35 of oxide over the gate electrode. Note how the oxide dimple slightly overlaps portions of the N+ regions that are proximate the trenches. The overlapping oxide dimple effectively reduces the surface area of the source regions and thereby increases the on resistance of the device. In contrast, the invention process ensures that the isolation regions are removed from the upper surface of the upper layer by providing that the isolation material in the trench is etched slightly below the upper surface of the upper layer. The invention has, in effect, a recessed or concave surface in the isolation material at the top of the trench in contrast to the overlapping, convex surface of Blanchard's dimple 35.

Temple does not show or suggest the invention. Temple has an oxide surface protruding above the upper surface of an upper layer. See, e.g. Fig. 3 where the oxide protrudes above the upper surface of upper layer 14.

The Japanese publication also fails to show or suggest the invention.

Applicants have distinguished their invention from the art of record. Consideration of this amendment and allowance are requested.

Respectfully submitted,

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